# Mark W. Wilson

**710 S.E. 34th Avenue, Portland, OR 97214**
**H:** 503.233.8867 **C:** 503.970.4625 **E:** mwilson@rdrop.com


## SUMMARY OF QUALIFICATIONS

- Eleven years of experience developing electronic design automation (EDA) physical design tools, methodology, and training, for three flagship architecture microprocessor designs.
- Strong technical analysis, problem solving skills, and experience managing complex, multi-site tasks.

## EDUCATION

**J.D., anticipated December 2008** — **LEWIS & CLARK LAW SCHOOL**
**GPA**: 3.40/4.0 **Class rank**: 50/264 — **PORTLAND, OR**
**ELECTRONIC RESOURCES EDITOR & MEMBER:** Environmental Law Review

**B.S., Electrical and Computer Engineering, May 1995** — **CARNEGIE MELLON UNIVERSITY, PITTSBURGH, PA**

*Channel Routing using Boolean Satisfiability*, independent senior project.
**Graduate Coursework**: *Finite Element Analysis I*, Columbia University, 1998.
*Algorithms for Design Automation II*, Portland State University, 1997.

## EXPERIENCE

### Intel Corp.

**Desktop Products Group** — **July 1995—Present**

*Senior Staff Design Automation Engineer* — December 2003—Present

- Automated standard cell library build flows, validation, data mining, and performed library design work for future 45 nm flagship microprocessor.
- Developed a revolutionary design tool allowing on-the-fly standard cell creation. This reduced standard cell concept-to-usage turnaround time from one-two months, to half a day.
- Invention disclosure reviewer for Intel Legal Software IP committee.

*Physical Design Automation Team Lead* — January 2000—December 2003

- Managed a team of six CAD engineers. Developed physical design tools and methodology for mixed cell-based/full-custom design style, 90 nm technology lead vehicle Pentium 4® microprocessor.
- Developed 90nm process standard cell library layout architecture specifications. Coordinated process design rule impact estimation between design & manufacturing process development groups.

*Staff Design Automation Engineer* — July 1995—January 2000

- Specified and implemented new design automation tools, scripts, and methodologies for Pentium II® and Pentium 4® processors. Applications support for Intel's custom layout editor and leaf cell layout synthesis tool, supporting over one hundred mask designers.
- Specified and directed development of Intel's first DFM, dummy metal fill and decoupling capacitor insertion tool. Built an automatic repeater station layout tool using IC Craftsman routing tool.

**CARNEGIE MELLON RESEARCH INSTITUTE** — **January 1992—May 1995**
Paid student internship. Designed, built, and tested industrial control and solid state gas sensor prototypes.

## AWARDS, ACTIVITIES, AND INTERESTS

INTEL DIVISION AWARD: Outstanding execution: Prescott A0 layout verification and tapeout/assembly.
INTEL DIVISION AWARD: Contributions in analysis, design, and implementation of fixes for Pentium 4® bin8 issue, resulting in 20 percent yield increase.
INTEL DIVISION AWARD: Development of incremental standard cell library methodology.
ALUMNUS REPRESENTATIVE: Carnegie Mellon Admissions Council, 1996-1999.
Avid road bicyclist, alpine skier, homebrewer, and BJCP National level beer judge.

## PUBLICATIONS

*Novel Features & Methodology to Increase Physical Design for Debug Coverage by 10X*, DTTC (*), 2003.
*Rapid Interconnect Design Through the Use of Virtual Repeaters*, DTTC, 2000.
*Willamette Stretchable Cell Layout Methodology*, DTTC, 1997.

*(*) Design & Test Technology Conference, Intel's EDA conference. Co-author on all papers listed.*